

What is claimed is:

1 1. A micro-leadframe for mounting at least one
2 integrated circuit, comprising:

3 a flat base having at least one conductive lead
4 pattern to provide electrically conductive paths for said at
5 least one integrated circuit; and

6 a plurality of preload extension tabs arranged
7 about said at least one conductive lead pattern, the preload
8 extension tabs protruding at an angle with respect to the
9 flat base to a predetermined height above the flat base.

1 2. The micro-leadframe of claim 1, wherein said at
2 least one integrated circuit is positioned on said at least
3 one conductive lead pattern of the flat base, said at least
4 one integrated circuit comprising a mold cap having a
5 predetermined height above the flat base.

1 3. The micro-leadframe of claim 2, wherein said at
2 least one integrated circuit package further comprises a
3 semiconductor die within the mold cap.

1 4. The micro-leadframe of claim 3, wherein the
2 semiconductor die comprises a flipchip die.

1 5. The micro-leadframe of claim 3, wherein the
2 preload extension tabs are directly connected to the mold
3 cap.

1 6. A micro-leadframe package, comprising:

2 a flat base having a conductive lead pattern;

3 an integrated circuit connected to the conductive
4 lead pattern of the flat base;

5 a plurality of preload extension tabs arranged
6 about the conductive lead pattern, the preload extension
7 tabs protruding at an angle with respect to the flat base
8 into the integrated circuit package to a predetermined
9 height above the flat base.

1 7. The micro-leadframe package of claim 6, wherein
2 the integrated circuit comprises a plastic mold cap having a
3 predetermined height above the flat base.

1 8. The micro-leadframe package of claim 7, wherein
2 the integrated circuit further comprises a semiconductor die
3 within the mold cap.

1 9. The micro-leadframe package of claim 8, wherein
2 said at least one integrated circuit package further
3 comprises a plurality of flipchip connections between the
4 semiconductor die and the conductive lead pattern.

1 10. The micro-leadframe package of claim 8, wherein
2 the preload extension tabs are directly connected to the
3 flat base.

1 11. A method of packaging an integrated circuit,
2 comprising the steps of:

3 providing a patterned micro-leadframe having a
4 flat base;

5 forming a plurality of preload extension tabs
6 protruding from the flat base at a predetermined angle with
7 respect to the flat base to a predetermined height above the
8 flat base; and

9 attaching a mold compound to the micro-leadframe.

1 12. The method of claim 11, further comprising the
2 step of providing a top mold platten.

1 13. The method of claim 12, wherein the step of
2 attaching the mold compound to the micro-leadframe comprises
3 the step of heating the top mold platten and forcing the top
4 mold platten against the preload extension tabs.

1 14. The method of claim 13, further comprising the
2 step of providing a bottom mold platten.

1 15. The method of claim 14, wherein the step of
2 attaching the mold compound to the micro-leadframe further
3 comprises the steps of heating the bottom mold platten and
4 pressing the bottom mold platten against the patterned flat
5 base.

